Hall Ticket Number:

Code No. : 21503

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. II Year (I.T.) I-Semester (Main) Examinations, December – 2015

Digital Electronics and Logic Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

Part-A (10 X 2=20 Marks)

1. The Decimal number -34 is expressed in 2's complement form as _____.
2. Show that NAND gate is an universal gate.
3. Simplify the Boolean function f = ((A'+B+C+D)'((ABC)'D))' using De Morgan's theorem.
4. Use a K-map to reduce the given Boolean expression to a minimum SOP form, f = ((AB)'+AB')(CD+C'D').
5. Realize a three input EX-NOR gate using two input NOR gates.
6. What are the asynchronous inputs to a flip-flop? How are they used?
7. Distinguish between Mealy and Moore state models.
8. Distinguish between a PLA device and a PAL device in terms of architecture.
9. An FSM circuit uses 10 states. Determine the minimum number of flip-flops required.
10. What is meant by "Configuration" in VHDL?

Part-B (5 X 10=50 Marks)

11. a) Draw the AND – OR gate implementation of the function $F(A,B,C,D) = \sum(0,2,5,6,7,8,10)$ after simplifying it in sum – of – products(SOP) form. [5]

    b) The dual of complement of a certain Boolean expression is given by ABC+D'E+BC'E. Find the expression. [5]

12. a) Design a 4bit comparator logic using logic gates. [6]

    b) Write a VHDL program to model a 16:1 MUX using 4:1 MUX blocks in structural modeling style. [4]

13. a) With the help of a logic diagram, describe the operation of a clocked R-S Flip-Flop with active LOW R and S inputs. Draw the truth table, if it were negatively edge-triggered. [5]

    b) Design a binary ripple counter that counts 000 and 111, and skips the remaining six states using JK flip flops with negative edge triggering. [5]

14. a) Design an FSM which can detect the sequence 0110, use D flip-flops. [6]

    b) Write a VHDL program to model a 4 bit UP-DOWN counter. [4]

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15. a) What is an ASM chart? Explain the building blocks of ASM chart. [5]

    b) Draw an ASM chart to design a binary Multiplier and describe the same. [5]

16. a) Convert the following decimal numbers to binary, octal and hexadecimal

    5, 100, 828 [4]

    b) Design a binary to gray code converter. [6]

17. Write short notes on any **two** of the following:

    a) Shift registers [5]

    b) FSM as an arbiter circuit [5]

    c) Digital Hardware design flow [5]